```
****************************************
Report : timing
        -path full
        -delay max
        -max_paths 1
        -sort_by group
Design : Johnson_count_1
Version: F-2011.09-SP2
Date   : Thu Jan 17 14:23:45 2013
****************************************

Operating Conditions: TYPICAL   Library: saed90nm_typ_ht
Wire Load Model Mode: enclosed

  Startpoint: out_reg[0] (rising edge-triggered flip-flop clocked by clk)
  Endpoint: out[0] (output port clocked by clk)
  Path Group: clk
  Path Type: max

  Des/Clust/Port     Wire Load Model       Library
  ------------------------------------------------
  Johnson_count_1    8000                  saed90nm_typ_ht

  Point                                    Incr       Path
  -----------------------------------------------------------
  clock clk (rise edge)                    0.00       0.00
  clock network delay (propagated)         0.05       0.05
  out_reg[0]/CLK (DFFARX1)                 0.00       0.05 r
  out_reg[0]/Q (DFFARX1)                   0.34       0.39 f
  out[0] (out)                             0.00       0.39 f
  data arrival time                                   0.39

  clock clk (rise edge)                   20.00      20.00
  clock network delay (propagated)         0.00      20.00
  clock uncertainty                       -0.40      19.60
  output external delay                   -8.00      11.60
  data required time                                 11.60
  -----------------------------------------------------------
  data required time                                 11.60
  data arrival time                                  -0.39
  -----------------------------------------------------------
  slack (MET)                                        11.21
```